Efficient method for the design of high-speed bipolar decision circuit

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Abstact

This paper presents an efficient method for speed performance optimisation of very high bit rate telecommunication circuits. The method uses predictive program for modelling of HBT transistors in function of technological and geometrical parameters and exploits analytical formulae for basic circuit performance. The design of a bipolar decision circuit is given as an example of the presented methodology.

Introduction

Rapid developments in semiconductor technologies, increasing complexities of circuits, higher integration levels open new perspectives for very high speed telecommunication networks. At the same time, new challenges for design methodologies appear. The design of digital circuits operating at 20 Gb/s rates and over is a very special task. Operating at the technology limits imposes harder demands on transistor models accuracy. Simulation must be realised taking into account analog effects. Placement and layout phase should be performed carefully, most often in full-custom mode, and parasitic effects should be backannoteted, resimulated and if necessary modified. Performance sensitivity to technological dispersions should be evaluated and taken into account in the design process.

Devices modelling

Reliable simulation of electronic circuits cannot be obtained without accurate models of circuit devices, and in particular semiconductor devices. This is especially relevant to IC technologies where post-fabrication tuning is extremely difficult, if possible at all. Devices models used in electrical simulators can be expressed in function of either electrical or technological and geometric parameters. The electrical parameters are very useful from the circuit design perspective, however, they are rather inconvenient from manufacturing point of view as they cannot provide the required feedback for process analysis and device design optimisation. A set of technological and geometric parameters is much more relevant to manufacturing process than a set of electrical parameters. Technological and geometric parameters are also much more convenient to impose technology constraints and analyse performance fluctuations due to variations of fabrication processes. They also ease the expression of statistical distributions and especially statistical correlations between parameters. Quite often a "mixed" set of parameters is used which includes electrical as well as technological and geometric parameters [1].

ACPAR2 program

ACPAR2 is a program, developed at Bagneux Laboratory, for optimising both the layer structure and transistor geometry. The program flowchart is presented in Fig.1. Input data are organised into two independent files : the *technological data* file and the *geometric data* file. The first file contains parameters relevant to the used technology such as layers dimensions, composition, doping levels. The second file contains transistor geometric parameters. The program has access to the material database containing necessary parameters of materials used. This program calculates a Gummel-Poon (Spice-type) model in function of technological and geometric data. It calculates also basic transistor performance such as e.g. Ft and Fmax at different current densities.

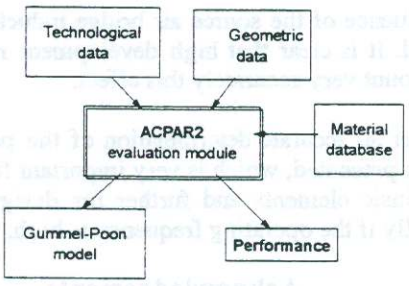

Fig.1 ACPAR2 flowchart

In Fig. 2 is presented a plot issued from ACPAR2 calculations. Ft of GaAs HBT are presented in function of Ic current and for different bias voltages Vce.

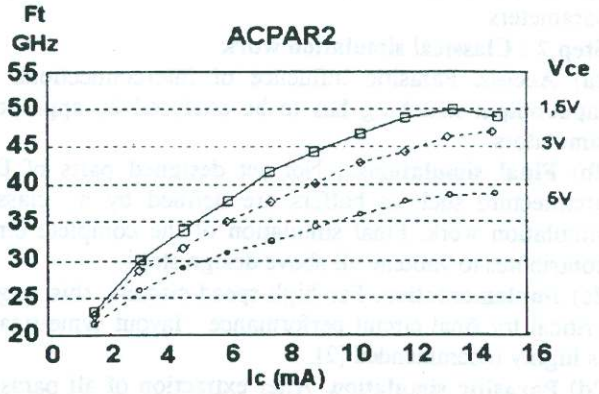

Fig.2 GaAs HBT: Ft in function of Ic and Vce

Lightwave communication network

Fig.3 shows the diagram of a ligthwave communication network. It consists in two parts : the emission and reception parts, transmission between them being performed by an optical fiber.

The emission part is composed of a multiplexer, a driver circuit for internal or external modulation of a laser diode : the electrical signal is converted to an optical signal by the laser diode itself.

A photo-element (currently a photodiode), placed in front of the reception part, converts an optical signal to an electrical one. Several amplifiers are used either to improve signal to noise ratio or to provide a constant voltage (e.g. AGC, Automatic Gain Control amplifier) at the input of the decision circuit (DEC). Driven by the clock recovery circuit, the decision circuit is used for restoring the signal on its logical levels (high and low) before demultiplexing. This circuit appears to be one of the most critical circuit to realise at high bit rate [2].

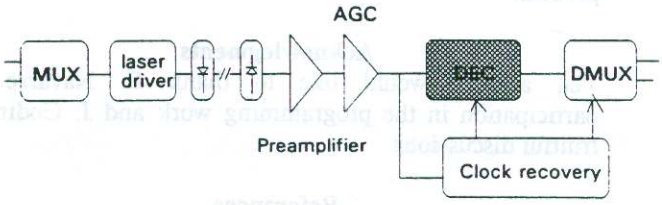

Fig.3 Lightwave transmission diagram.

Circuit definition and evaluation

In this paper, we concentrate on different design aspects of a decision circuit. At first, we define its architecture as simple and performing as possible, such as the serial approach [3]. It consists in a D flip-flop pre and post - buffered (see Fig. 4), respectively used for decision operation (MSFF), sensitivity improvement (input buffer) and external impedance matching (output buffer).

Fig.4 Block diagram of a serial decision circuit

We propose a circuit performance evaluation based on analytical expression of the propagation delay time in an ECL gate [4] corrected for the serial gating structure of the flip-flop and expressed in function of the circuit parameters such as logical swing SW, base resistance Rb, load resistance Rl, cut-off (Ft) and maximal oscillation (Fmax) frequencies of transistors used. Thus, the maximal bit rate Dmax can be expressed as :

$$Dmax = K \cdot Ft \quad (1)$$

where :

$$K = 1.8/\left[1+6.7(SW/x)+0.645(1+x)y^2\right] \quad (2)$$

with :

x : resistances Rl/Rb ratio (also equal to m/Ic)

y : transistor Ft/Fmax ratio (depending on Rb.Cbc product)

m : swing / base resistance ratio

Ic : operation current

This evaluation, given for a logical swing SW and different values of Ft/Fmax, is convenient for any serial decision circuit. Coefficient K, for a logical swing of 0.4V, is presented in Fig. 5. The maximal bit rate can be obtained, for given Ft and Fmax, by adapting the "optimal" load resistance Rl to the transistor base resistance Rb, with regard to current density (Fig.2).

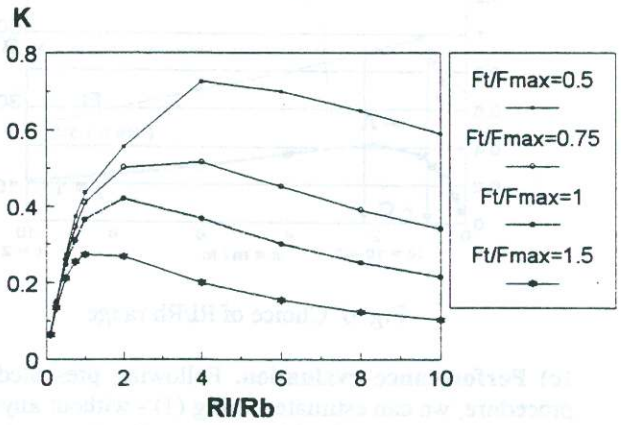

Fig.5 Coefficient K

Design method

ACPAR2 program, determining Ft and Fmax, and circuit formulae, enabling to choose the best ratio Rl/Rb for a given Ft/Fmax ratio, coupled together, allow to determine rapidly the maximal bit rate, given by (1), of the decision circuit in function of physical parameters. Sensitivity to

parameter dispersion can also be estimated. This methodology allows to estimate technology possibilities, decide on a choice of circuit architecture, perform some basic parameter optimisation without time consuming SPICE simulations, and moreover evaluate circuit performance once the parameters of fabricated devices are known.

Design method illustration

Objective. The above methodology is applied to the design of a 20 Gb/s decision circuit using a GaAs bipolar technology (HBT with Ft = Fmax = 50 GHz).

Procedure.

Step1 : Pre-determining choices

1a) **Transistor choice**. First of all, the transistors performance are analysed by ACPAR2 for a current density range. This analysis gives both the Ft/Fmax ratios and the optimal operation current for each transistor geometry. Based on this data, optimal transistor(s) geometry can be chosen.

1b) **Load resistance choice.** Three criteria must be taken into account : i) the internal logical swing value, ii) Ft versus current density (see Fig. 2), iii) Dmax versus Rl/Rb (see Fig. 5). It clearly appears that a compromise has to be found.

We proceed as follows : after having chosen a nominal value for logical swing, we can gather Fig 2 and convenient curve of Fig 5 by expressing Ft and K in function of m/Ic, what gives Fig 6. We successively determine K (see A), the minimal Ft value to obtain the required bit rate by using (1), the convenient current density range (see B) and finally the appropriate Rl/Rb (see C) and nominal current ranges.

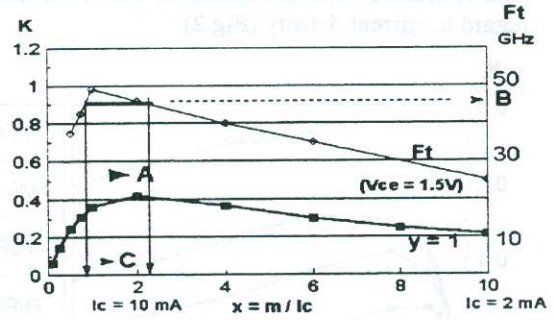

Fig. 6 Choice of Rl/Rb range

1c) **Performance evaluation.** Following presented above procedure, we can estimate - using (1) - without any SPICE simulation, the maximal bit rate. In the discussed case, a maximal bit rate slightly above 20 Gb/s can be expected with Rl/Rb close to 2, for a serial DEC architecture.

1d) **Sensitivity study.** ACPAR2 can once more be exploited to evaluate the sensitivity to some critical technological parameters. Centring Rl value can protect circuit performance against dispersion of technologica parameters.

Step 2 : Classical simulation work

2a) **Access.** Parasitic influence of interconnections and input/output matching has to be analysed by appropriate simulators.

2b) **Final simulations.** Not yet designed parts of DEC architecture such as buffers are defined by a classical simulation work. Final simulation of the complete circuit contributes to validate all above design steps.

2c) **Implementation.** For high speed circuits, this stage is critical for final circuit performance : layout symetrization is highly recommended [2].

2d) **Parasitic simulation.** After extraction of all parasitics from layout, parasitic simulation allows to predict the upper limit operation. Fig. 7 gives a simulated eye diagram at 20 GB/s in case of the discussed design.

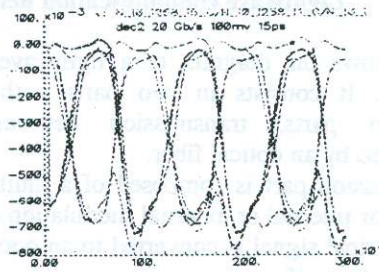

Fig. 7 Simulated eye diagram of a DEC at 20 GB/s

Conclusion

An efficient method has been presented for the design of lightwave transmission circuits such as the decision circuit. It is based on use of ACPAR2 program coupled to bit rate performance predicting formulae. As shown on an example, this approach can drastically reduce simulation time and ease some determining choices during design process.

Acknowlegments

The authors would like to thank E. Navarre for participation in the programming work and J. Godin for fruitful discussions.

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